IN THE SPECIFICATION

The applicant files replacements for paragraphs 9, 11, 14, 15, 16 of the specification in compliance with 37 CFR 1.121 without introducing new matter.

[0009] A field effect transistor 200 in accordance with an embodiment of the present invention is illustrated in Figure 2. Field effect 200 is formed on an insulating substrate 202. In an embodiment of the present invention, insulating substrate 202 includes an insulating film 204 grown on a substrate 206. In other embodiments, other types of insulating substrates, such as but not limited to ~~hafium~~ hafnium (Hf) oxide, zirconium oxide, and barium titanate ($BaTiO_3$) may be used.

[0011] Transistor 200 has a gate dielectric 210 formed on the thin film channel region 208. Although the gate dielectric 210 can be a grown dielectric, such as SiO_2 or silicon oxynitride, the gate dielectric is preferably a deposited dielectric so that it can be formed at lower temperatures, less than 500°C, and thereby be compatible with the narrow bandgap channel region film (e.g. InSb). In an embodiment of the present invention, the gate dielectric 210 is or includes a high dielectric constant film. A high dielectric constant film has a dielectric constant of greater than 9.0 and ideally greater than 50. A high dielectric constant film can be a metal oxide dielectric, such as but not limited to tantalum pentaoxide (Ta_2O_5), titanium oxide, ~~hafium~~ hafnium (Hf) oxide, zirconium oxide, and aluminum oxide. The gate dielectric layer 210, however, can be other well known high dielectric constant films, such as lead zirconate titanate (PZT) or barium strontium ~~titatanate~~ titanate (BST). Utilizing a high dielectric constant film enables a gate dielectric to be formed relatively thick between 20-3000A and

ideally about 200A for a high dielectric constant (k > 100) material. A thick gate dielectric layer helps block gate leakage current of the device. Any well known techniques, such as vapor deposition or sputtering can be used to deposit gate dielectric film 210. In an embodiment of the present invention, a low temperature process, between 200-500°C, is used to deposit the gate dielectric.

[0014] In an embodiment of the present invention, the source region 220 and the drain region 222 are formed of materials which ~~surpress~~ suppress parasitic transistor leakage due to the low bandgap of the channel region. In an embodiment of the present invention, the source region 220 and drain regions 222 are formed from a wide or high bandgap semiconductor material. When forming the source 220 and drain 222 region from a semiconductor material, the bandgap of the semiconductor film of the source 220 and drain 222 regions should have a bandgap which is greater than the bandgap of the channel region. In an embodiment, the bandgap of the source and drain semiconductor material is at least 0.2 eV and ideally at least 0.5 eV greater than the bandgap of the semiconductor film 208 in the channel region. The bandgap offset between the source/drain semiconductor 220 and 222 film and the channel semiconductor film 208 prevents carrier injection over the barrier. In an embodiment of the present invention, the source region 220 and drain region 222 are formed from a III-V compound semiconductor having a larger band gap compared to the channel region semiconductor, such as but not limited to InP (Bandgap = 1.35 eV), GaSb (Bandgap =0.75 eV), GaP, and GaAs (Bandgap=1.43). However, other semiconductor materials, such as germanium (Bandgap = 0.67) having a suitably large bandgap can be used. The source/drain semiconductor film can be a polycrystalline film or a single crystalline semiconductor film 220 and 222 can be doped to a concentration level between $1x10^{20} - 1x10^{21}$ atoms/cm^3 with n type

impurities, such as arsenic, antimony or phosphorous in order to form a n type MOS device (NMOS) and can be doped to a concentration level between $1x10^{20}$ – $1x10^{21}$ atoms/cm^3 with p type impurities, such as boron or gallium when forming a p type device (PMOS). By forming the source 220 and drain 222 regions with a wide or large bandgap material and placing them next to the narrow or small bandgap channel region 208 a barrier is created which suppresses parasitic transistor leakage which would normally occur with a low bandgap channel region.

[0015] In another embodiment of the present invention, the source region and drain regions are formed from a metal film. In an embodiment of the present invention, the source and drain regions are formed from a metal ~~or~~ film ("Schottky metal'), such as but not limited to platinum (Pf), aluminum (Al) and gold (Au) which can form a "Schottky" barrier with the semiconductor film of the channel region 208. The "Schottky" barrier which is created by placing the metal source and drain regions in contact with the semiconductor film of the channel region forms a barrier to electric flow from the source and drain regions into the channel region. In this way, a bias is needed in order to inject carriers from the source 220 and drain 222 into the channel 208. In an embodiment of the present invention, the source region and drain regions are formed from a metal film, such as but not limited to titanium nitride (TiN), tantalum nitride (TaN) and ~~hafium~~ hafnium nitride (HfN).

[0016] The use of an insulating substrate and special band engineered source/drain regions ~~surpresses~~ suppresses parasitic transistor leakage due to the low bandgap of the channel region material (e.g., InSb). In this way, transistor 200 can function as a low power, high performance device.